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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,260	08/30/2000	Jong Sang Baek	8733.A285	1251

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EXAMINER	
NGUYEN, KIMNHUNG T	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 03/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,260	BAEK, JONG SANG	
	Examiner	Art Unit	
	Kimnhung Nguyen	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 6-8* is/are rejected.

7)☒ Claim(s) *4,5,9 and 10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Application has been examined. The claims 1-10 are pending. The examination results are as following.

Claim Objections

1. Claim 7, lines 8, after "first controller", should delete --first controller--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3 and 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shyu et al. (US 5,486,868) in view of Matsueda (US 6,873,312).

Regarding claim 1, Shyu et al. discloses in fig.1, a display mode system with a multi-timing controller comprising a display standard (see video scan modes, fig. 2); an interface receiving a timing data inputted from the exterior thereof and a control signal corresponding to the display standard; a timing controller (10) for latching and outputting the timing data inputted from the interface, and for generating and outputting timing signals for driving based on the control signal (121); and a driving circuit (fig. 1) for receiving the timing signals outputted from the timing controller to display a picture corresponding to the display standard, wherein the timing controller (10) includes a decoder (12) and a timing generator (13), wherein timing

generation information corresponding to a plurality of display standards is stored by the decoder (see col. 2,lines 54-60), wherein the decoder (12) may output to the timing generator (horizontal timing generator 14), timing information corresponding to the timing data, and wherein timing generator outputs timing signals corresponding to the timing information and the control signal (see col.3, lines 5-20), and wherein the timing generator (14) includes a first controller (15) for generating the timing signal corresponding to the timing information selected from the decoder and a second controller (16) for generating a gate drive starting signal from one vertical synchronizing signal (see fig. 5).

However, Shyu et al. does not disclose the display device is a liquid crystal display, and a second controller for generating a liquid crystal polarity inversion signal indicating a driving voltage polarity.

Matsueda discloses in fig. 6, the display device is a liquid crystal display (see abstract) and a second controller (D/A converter) for generating a liquid crystal polarity inversion signal indicating a driving voltage polarity (see col. 11, lines 29-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the display device is a liquid crystal display, and a second controller for generating a liquid crystal polarity inversion signal indicating a driving voltage polarity as taught by Matsueda into the system of Shyu et al. because this would provide the D/A it self in this method, which is not to provide data wiring in multiple system, the circuit at a high speed is not required, and the current consumption is low (see col. 11, lines 19-23).

Regarding claim 2, Shyu et al. discloses further the display comprising a dip switch (see pixel clock131) for selecting the timing data corresponding to the display standard.

Regarding claim 3, Shyu et al. discloses the decoder (12) consist of a memory for storing a certain timing information and a multiplexor (MUX 19) for selecting any of the timing information stored in the memory (see col. 2, lines 54-60).

Regarding claim 6, Shyu et al. discloses the display standard is selected from VGA (see display mode of fig. 2).

Regarding claim 7, Shyu et al. discloses in fig. 1, a multi-timing controller, comprising a decoder (12) for storing timing generation information corresponding to a plurality of display standard (see col. 2, lines 54-60), wherein the decoder (12) is connected to a source outputting; and a timing generator (14) connected to an output of the decoder and to a source outputting a control signal (121) and to a source outputting a control signal corresponding to one of the plurality of display standards, wherein the timing generator outputs, to a display device, timing signals corresponding to an output of the decoder and the control signal (121), wherein the timing generator includes a first controller (15) that generates the timing signal output by the timing generator and a second controller (16) for generating a gate drive starting signal from one vertical synchronizing signal (see fig. 5).

However, Shyu et al. does not disclose the display device is a liquid crystal display, and a second controller for generating a liquid crystal polarity inversion signal indicating a driving voltage polarity.

Matsueda discloses in fig. 6, the display device is a liquid crystal display (see abstract) and a second controller (D/A converter) for generating a liquid crystal polarity inversion signal indicating a driving voltage polarity (see col. 11, lines 29-40) as discussed above.

Regarding claim 8, Shyu et al. discloses the decoder includes a memory and a Multiplexor (19, see fig. 1, see col. 2, lines 54-60).

Allowable Subject Matter

4. Claims 4-5 and 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The present invention is directed a liquid crystal display device with a multi-timing controller comprising a liquid crystal display panel having a display standard receiving a timing data inputted from the exterior thereof and a control signal corresponding to the display standard; a timing controller for latching and outputting the timing data inputted from the interface, and for generating and outputting timing signals for driving the liquid crystal display panel based on the control signal; and a driving circuit for receiving the timing signals outputted from the timing controller to display a picture corresponding to the display standard, wherein said timing controller includes a decoder, and a timing generator, wherein timing generation information corresponding to a plurality of display standards is stored by the decoder. The combination of

Shyu et al. (US 5,486,868), Schiefer et al. (US 6,177,922) and Barshinger (US 5,049,864) show a similar system having multi-timing controller and a plurality of display standards is stored by a decoder. However, they fail to teach that the timing generator includes a first controller for generating the timing signal corresponding to the timing information selected from the decoder, a third controller for generating a signal information a sampling start of a data and source sampling clock for latching a data at the rising or falling edge during one horizontal synchronization period; a fourth controller for deforming a gate output enable signal generated from the first controller by making the gate output enable signal into a high state during a certain time so as to prevent a latch-up badness in which all the outputs of a gate drive integrate circuit goes to a high state, thereby disabling the gate drive integrated circuit; and a fifth controller for always equally keeping the polarity of the horizontal/vertical synchronizing signal as claims 4 and 9; or a fourth comparator for comparing the second count value with a fourth timing information inputted from the decoder to output a fourth selection timing signal when the two input values are equal; a fifth comparator for comparing the second count value with a fifth timing information inputted from the decoder to output a fifth selection timing signal when the two input values are equal; and sixth comparator for comparing the second count value with a sixth timing information inputted from the decoder to output a sixth reference timing signal when the two input values are equal as claim 5.

Response To Arguments

5. Applicant's arguments with respect to claims 1-10 filed on 12/14/05 have been considered but are moot in view of the new ground(s) of rejection.

Applicant states that Shyu does not teach "wherein the timing generator includes a first controller that for generating the timing signal corresponding to the timing information selected from the decoder and a second controller for generating a liquid crystal polarity inversion signal indicating a driving voltage polarity of the liquid crystal provided on the liquid crystal panel and a gate drive starting signal for notifying a first drive line of a field form one vertical synchronizing signal".

Examiner disagrees because Matsueda does disclose the limitations in fig. 6, and discussed above.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimnhung Nguyen whose telephone number is (571) 272-7698. The examiner can normally be reached on MON-FRI, FROM 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kimnhung Nguyen

March 1, 2006

PATRICK N. EDOUARD
SUPERVISORY PATENT EXAMINER